

WHAT IS CLAIMED IS:

1. A parallel pattern detection engine (PPDE) integrated circuit (IC) for detecting one or more patterns in a sequence of input data comprising:

- an input/output (I/O) interface for coupling data into and out of the PPDE;
- M processing units (PUs), each of the M PUs having compare circuitry for comparing each of the sequence of input data to a pattern stored in each of the M PUs and generating a compare output, wherein an address pointer selecting the pattern in each of the M PUs is modified in response to a logic state of the compare output and an operation code stored with the pattern;
- an input bus for coupling the sequence of input data to each of the M PUs in parallel;
- an output bus coupled to the I/O interface for sending output data to the I/O interface;
- control circuitry coupled to the I/O interface and coupling control data on a control data bus and identification (ID) on an ID bus to each of the M processing units;
- ID selection circuitry for selecting a match ID from ID data identifying the M PUs in response to a pattern match signal and match mode data, wherein the match ID and match data corresponding to the match ID are saved in a temporary register as the output data; and
- cascade circuitry coupled from each of the M PUs to one or more adjacent PUs within the M PUs for selectively coupling chain data between one or more groups of two or more adjacent PUs selected from the M PUs in response to the control data.

1 2. The PPDE of claim 1 further comprising an input buffer coupled to the I/O
2 interface for receiving and writing input data as parallel data at a write address.

1 3. The PPDE of claim 2 further comprising a multiplexer coupled to the input
2 bus and the input buffer for sequentially coupling single data from the input buffer
3 data to the input bus, wherein parallel data are selected using a read address.

1 4. The PPDE of claim 1 further comprising an output buffer coupled to the
2 output bus and to the temporary register for receiving and writing output data to the
3 output buffer at a write address and coupling output data to the output bus
4 corresponding to a read address.

1 5. The PPDE of claim 1, wherein each of M processing units (PUs) has an ID
2 register for storing a unique ID sent from the control circuitry.

1 6. The PPDE of claim 1, wherein each of M processing units (PUs) has a control
2 register for storing the match mode data, wherein the match mode data determines
3 criteria for generating the match signal and the match data.

1 7. The PPDE of claim 1, wherein each of the M PUs has a memory register array
2 for storing a sequence of the pattern and corresponding operation codes addressed by
3 an address register indexed by the address pointer.

1 8. The PPDE of claim 1, wherein the cascade circuitry enables the stored
2 patterns of two or more PUs to be chained together as a single pattern using the chain
3 data.

1 9. The PPDE of claim 9, wherein the chain data inhibits indexing the pointer of
2 one PU until an adjacent PU coupled with the cascade circuitry has compared a last
3 pattern to an input data.

1 10. The PPDE of claim 1, wherein the compare circuitry in each of the M PUs
2 completes a compare of an input data to a selected pattern and generates a compare
3 output and modifies the address pointer in the same cycle of a clock signal.

1 11. The PPDE of claim 1, wherein the match mode data for each of the M PUs
2 sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly,

5 a longest match mode wherein a pattern match indicates that a particular
6 sequence of pattern corresponding to the match ID has the largest number of data in a
7 sequence that compared to a sequence of data in the sequence of input data wherein
8 the match data indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern bytes corresponding to the match ID has the largest number of
11 data that compared in a broken sequence that compared to a broken sequence of input
12 data, wherein the match data indicates the value of the largest number; and

13 a fuzzy match mode, wherein a pattern match indicates that a particular
14 sequence of pattern corresponding to the match ID has the closet match to the
15 sequence of input data as determined by a distance value, wherein the match data
16 indicates the distance value.

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1 12. The PPDE of claim 1, wherein the operation codes are selected from a set of
2 operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if
4 the compare output is a logic one and the address pointer is reloaded to its initial
5 value if the compare output is a logic zero;

6 an inverse operation code indicating that the address pointer is to be
7 incremented if the compare output is a logic zero and the address pointer is reloaded
8 to its initial value if the compare output is a logic one;

9 a wildcard operation code indicating that the address pointer is incremented if
10 the compare output is a logic zero or a logic one;

11 a multiple wild card operation code indicating that the address pointer is to be
12 held if the compare output is a logic zero otherwise the address pointer is
13 incremented; and

14 a last operation code indicating that the address pointer is frozen until the
15 matching process receives a reset if the compare output is a logic one and the address
16 pointer is reloaded to its initial value if the compare output is a logic zero.

1 13. The PPDE of claim 1, wherein bits of the selected pattern are masked by a
2 mask data stored in a mask register when the selected pattern is compared to an input
3 data, the mask data indicating which bits of the selected pattern are not compared.

1 14. A method of determining if any of N sequences of pattern occurs within a
2 sequence of input data using a parallel pattern detection engine (PPDE) comprising
3 the steps of:

4 a) loading the N sequences of pattern into M processing units (PUs), each of
5 the M PUs having compare circuitry for comparing each of the sequence of input
6 data, in parallel, to a selected pattern in each of the N sequences of pattern stored in
7 the M PUs;

8 b) loading identification (ID) data into each of the M PUs, wherein the ID data
9 determines an ID for each of the M PUs;

10 c) loading match mode data into each of the M PUs setting criteria for
11 determining when conditions have been met for indicating that one of the N
12 sequences of pattern has been detected in the sequence of input data;

13 d) coupling a first input data in parallel to each of the M PUs;

14 e) comparing the first input data to the selected pattern determined by an
15 address pointer in each of the M PUs and generating a compare output in each of the
16 M PUs within a same clock cycle;

17 f) modifying the value of the address pointer in each of the M PUs in response
18 to a logic state of the corresponding compare output and an operation code stored
19 with the selected pattern in each of the M PUs;

20 g) selecting a match ID from the ID data in response to a pattern match signal
21 indicating one of the N sequences of pattern has been detected;

22 h) storing the match ID and match data corresponding to the match ID; and

23 i) repeating steps (a-g) until a last input data of the sequence of input data has
24 been compared.

1 15. The method of claim 14, wherein cascade circuitry is coupled from each of the
2 M PUs to one or more adjacent PUs within the M PUs for selectively coupling chain
3 data between two or more adjacent PUs selected from the M PUs in response to
4 control data loaded into the two or more adjacent PUs.

1 16. The method of claim 14, one of the N sequences of pattern are partitioned and
2 loaded into the two or more M PUs.

1 17. The method of claim 14, wherein each of M processing units (PUs) has a
2 control register for storing the match mode data, wherein the match mode data
3 determines criteria for generating the match signal and the match data.

1 18. The method of claim 17, wherein each of the M PUs has a memory register
2 array for storing a sequence of the pattern and corresponding operation codes
3 addressed by an address register indexed by the address pointer.

1 19. The method of claim 15, wherein the cascade circuitry enables the stored
2 patterns of two or more PUs to be chained together as a single pattern using the chain
3 data.

1 20. The method of claim 19, wherein the chain data inhibits indexing the pointer
2 of one PU until an adjacent PU coupled with the cascade circuitry has compared a last
3 pattern to an input data.

1 21. The method of claim 14, wherein compare circuitry in each of the M PUs
2 completes a compare of an input data to a selected pattern and generates a compare
3 output and modifies the address pointer in the same cycle of a clock signal.

1 22. The method of claim 14, wherein the match mode data for each of the M PUs
2 sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly;

5 a longest match mode wherein a pattern match indicates that a particular
6 sequence of pattern corresponding to the match ID has the largest number of data in a
7 sequence that compared to a sequence of data in the sequence of input data wherein
8 the match data indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern corresponding to the match ID has the largest number of data that
11 compared to a broken sequence of input data, wherein the match data indicates the
12 value of the largest number;

13 a fuzzy match mode, wherein a pattern match indicates that a particular
14 sequence of pattern corresponding to the match ID has the closet match to the
15 sequence of input data as determined by a distance value, wherein the match data
16 indicates the distance value.

1 23. The method of claim 18, wherein the operation codes are selected from a set
2 of operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if
4 the compare output is a logic one and the address pointer is reloaded to its initial
5 value if the compare output is a logic zero;

6 an inverse operation code indicating that the address pointer is to be
7 incremented if the compare output is a logic zero and the address pointer is reloaded
8 to its initial value if the compare output is a logic one;

9 a wildcard operation code indicating that the address pointer is incremented if
10 the compare output is a logic zero or a logic one;

11 a multiple wildcard operation code indicating that the address pointer is to be
12 held if the compare output is a logic zero otherwise the address pointer is
13 incremented; and

14 a last operation code indicating that the address pointer is frozen until the
15 matching process receives a reset if the compare output is a logic one and the address
16 pointer is reloaded to its initial value if the compare output is a logic zero.

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1 24. A data processing system comprising:
2 a central processing unit (CPU);
3 a random access memory (RAM);
4 one or more parallel pattern detection engines (PPDEs); and
5 a bus coupling the CPU, RAM, and the one or more PPDEs, wherein each of
6 the PPDEs has an input/output (I/O) interface for coupling data into and out of the
7 PPDE;
8 M processing units (PUs), each of the M PUs having compare circuitry for
9 comparing each of the sequence of input data to a pattern stored in each of the M PUs
10 and generating a compare output, wherein an address pointer selecting the pattern
11 data in each of the M PUs is modified in response to a logic state of the compare
12 output and an operation code stored with the pattern data;
13 an input bus for coupling the sequence of input data to each of the M PUs in
14 parallel;
15 an output bus coupled to the I/O interface for sending output data to the I/O
16 interface;
17 control circuitry coupled to the I/O interface and coupling control data on a
18 control data bus and identification (ID) on an ID bus to each of the M processing
19 units;
20 ID selection circuitry for selecting a match ID from ID data identifying the M
21 PUs in response to a pattern match signal and match mode data, wherein the match ID
22 and match data corresponding to the match ID are saved in a temporary register as the
23 output data; and
24 cascade circuitry coupled from each of the M PUs to one or more adjacent
25 PUs within the M PUs for selectively coupling chain data between one or more

26 groups of two or more adjacent PUs selected from the M PUs in response to the
27 control data.

1 25. The data processing system of claim 24, wherein each of M processing units
2 (PUs) has an ID register for storing a unique ID sent from the control circuitry.

1 26. The data processing system of claim 24, wherein each of the M PUs has a
2 memory register array for storing a sequence of the pattern and corresponding
3 operation codes addressed by an address register indexed by the address pointer.

1 27. The data processing system of claim 24, wherein the cascade circuitry enables
2 the stored patterns of two or more PUs to be chained together as a single pattern using
3 the chain data.

1 28. The data processing system of claim 27, wherein the chain data inhibits
2 indexing the pointer of one PU until an adjacent PU coupled with the cascade
3 circuitry has compared a last pattern to an input data.

1 29. The data processing system of claim 24, wherein the compare circuitry in each
2 of the M PUs completes a compare of an input data to a selected pattern and generates
3 a compare output and modifies the address pointer in the same cycle of a clock signal.

1 30. The data processing system of claim 24, wherein the match mode data for
2 each of the M PUs sets a match mode comprising:

3 an exact match mode, wherein a pattern match indicates that the sequence of
4 pattern matches a sequence of input data exactly;

5 a longest match mode wherein a pattern match indicates that a particular
6 sequence of pattern corresponding to the match ID has the largest number of data in a

7 sequence that compared to a sequence of data in the sequence of input data wherein
8 the match data indicates the value of the largest number;

9 a maximum match mode, wherein a pattern match indicates that a particular
10 sequence of pattern corresponding to the match ID has the largest number of data
11 that compared to a broken sequence of input data, wherein the match data indicates
12 the value of the largest number; and

13 a fuzzy match mode, wherein a pattern match indicates that a particular
14 sequence of pattern corresponding to the match ID has the closet match to the
15 sequence of input data as determined by a distance value, wherein the match data
16 indicates the distance value.

1 31. The data processing system of claim 30, wherein the operation codes are
2 selected from a set of operation codes comprising:

3 a match operation code indicating that the address pointer is incremented if
4 the compare output is a logic one and the address pointer is reloaded to its initial
5 value if the compare output is a logic zero;

6 an inverse operation code indicating that the address pointer is to be
7 incremented if the compare output is a logic zero and the address pointer is reloaded
8 to its initial value if the compare output is a logic one;

9 a wildcard operation code indicating that the address pointer is incremented if
10 the compare output is a logic zero or a logic one;

11 a multiple wildcard operation code indicating that the address pointer is to be
12 held if the compare output is a logic zero otherwise the address pointer is
13 incremented; and

14 a last operation code indicating that the address pointer is frozen until the
15 matching process receives a reset if the compare output is a logic one and the address
16 pointer is reloaded to its initial value if the compare output is a logic zero.

- 1 32. The data processing system of claim 30, wherein bits of the selected pattern
- 2 are masked by a mask data stored in a mask register when the selected pattern is
- 3 compared to an input data, the mask data indicating which bits of the selected pattern
- 4 are not compared.